

E.E. 432.3

VLSI Circuit Design

Instructor: R.J. Bolton

MID-TERM EXAMINATION

February 10, 2004

5:30 PM - 7:00 PM

STUDENT NAME: _____

STUDENT NUMBER: _____

Question 1	/ 15
Question 2	/ 15
Question 3	/ 15
TOTAL	/ 45

GENERAL INSTRUCTIONS FOR THE QUESTIONS

- 1) OPEN E.E. 432.3 textbook (**Principles of CMOS VLSI Design - A Systems Perspective by N.H.E. Weste and K. Eshraghian OR one other text**), OPEN E.E. 432.3 notes, and OPEN E.E. 432.3 assignments.
- 2) NO library manuals (or copies thereof) ALLOWED! NO examination files ALLOWED!
- 3) Neatness counts. Please ensure your paper is readable.
- 4) Some questions contain special instructions. Please ensure that you read these carefully.
- 5) Not all questions are of the same difficulty and value. Consider this when allocating time for the solution.
- 6) *IF A QUESTION PROVES TO BE TOO HARD FOR YOU TO SOLVE, GO ON TO ANOTHER QUESTION! RETURN TO THE TROUBLESOME QUESTION WHEN TIME PERMITS.*

PLEASE NOTE

ALL parts of the examination paper MUST be handed in before leaving.

Please check that your examination paper contains 8 pages TOTAL.

SPECIFIC INSTRUCTIONS FOR THE EXAMINATION

- 1) All designs use standard CMOS3DLM design rules and layers. $V_{DD} = +5V$ and $V_{SS} = 0V$.
- 2) Unless otherwise specified, normal substrate connections are assumed for all P-channel and N-channel transistors, i.e., V_{SS} for N-channel and V_{DD} for P-channel.
- 3) CMOS3DLM resistance and capacitance parameters are as follows:

Layer	Resistance	Capacitance
N-Diffusion	25.0 Ω/\square	4.4E-4 pf/ μm^2
P-Diffusion	80.0 Ω/\square	1.5E-4 pf/ μm^2
Polysilicon	18.0 Ω/\square	6.0E-5 pf/ μm^2
Metal 1	0.035 Ω/\square	2.7E-5 pf/ μm^2
Metal 2	0.030 Ω/\square	1.4E-5 pf/ μm^2
N-Transistor	4275 Ω/\square	See below
P-Transistor	13600 Ω/\square	See below
Gate-channel	See above	6.9E-4 pf/ μm^2

- 4) Supplementary physical constants are as follows:

Constant	Symbol	Value	Units
Electron charge	q	1.602E-19	coulomb
Boltzmann's constant	k	1.38E-23	Joule/ $^{\circ}K$
Intrinsic carrier concentration of Si @ T=300 $^{\circ}K$ (27 $^{\circ}C$)	n_i^2	2.1E+20	(carriers/cm ³) ²
Permittivity of free space	ϵ_0	8.854E-14	Farad/cm
Permittivity of Si	ϵ_{Si}	11.7 ϵ_0	Farad/cm
Permittivity of SiO ₂	ϵ_{ox}	3.9 ϵ_0	Farad/cm

- 5) (H)SPICE process parameters are as follows:

Parameter	Name	N-channel	P-channel	Units
V_t	Zero-bias threshold voltage	0.7	-0.8	Volts
κ'	Process gain factor	40.0E-6	12.0E-6	A/V ²
γ	Bulk threshold body factor	1.1	0.6	V ^{1/2}
$2 \phi_F $	Surface potential	0.6	0.6	V
λ	Channel length modulation factor	1.0E-2	3.0E-2	1/V
t_{ox}	Oxide thickness	5.0E-6	5.0E-6	cm
N_A or N_D	Substrate doping density	1.7E+16	5.0E+15	1/cm ³
m	Carrier surface mobility	775	250	cm ² /(V·sec)

QUESTION #1**MARKS: 15 (3 + 3 + 3 + 3 + 3)**

Indicate (in the space provided) whether the following are TRUE or FALSE. **Do any FIVE (5).** To obtain full marks for each question, include a **SHORT** sentence or two in support of your answer.

_F__ 1) The CMOS3DLM design rule for the enclosure of P-Well and n-transistor is 3 design scale microns (dsm).

False. The 3 dsm rule (C.3) refers to diffusion (device well). A transistor would include the gate area. Therefore the distance is 7 dms (C.4)

_F__ 2) The P+ mask patterns where the device wells of the p-transistors will be.

False. The device wells (thin-ox) are patterned by the device well mask. The P+ mask patterns the P+ implant areas (which surround some of the device wells).

_T__ 3) The input gate capacitance of an E.E. 432.3 minimum size inverter (MSI) is approximately 24.84fF.

True. From page 2, the channel (i.e., gate) capacitance is $6.9 \times 10^{-4} \text{pF}/\mu\text{m}^2$. Since a MSI has 4 of C_g and 1 of C_g is $3\mu\text{m} \times 3\mu\text{m}$ then the capacitance is $(4) \times (9\mu\text{m}^2) \times 0.69\text{fF}/\mu\text{m}^2 = 24.84\text{fF}$.

_F__ 4) The Nortel Office of Technology at the Canadian Microelectronics Corporation (CMC) is the silicon broker (i.e., arranges fabrication) for the University of Saskatchewan.

False. There is no Nortel Office of Technology (NOT) at the CMC. The VLSIIC does the brokering (arranges fabrication).

_F__ 5) The circuit shown in Question #2 has three (3) transmission gates in it.

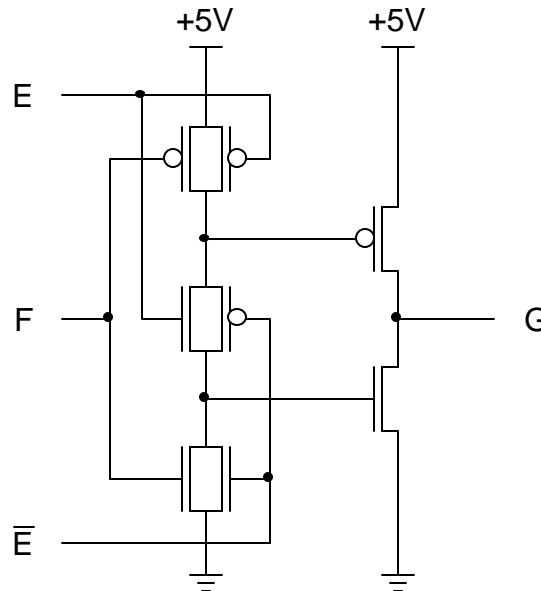
False. A transmission gate consists of a n-channel transistor in parallel with a p-channel transistor. Therefore there is only 1 transmission gate in the circuit.

T/F 6) Sequential logic must be used at a minimum frequency of approximately 1kHz.

True. If the sequential logic is dynamic.
False. If the sequential logic is static.

QUESTION #2**MARKS: 15 (10 + 5)**

Consider the following schematic diagram of a CMOS circuit.



- a) Using the following standard colors, draw a STICKS diagram of the circuit, as shown above. Use the following page. Note: Do NOT use Metal 2 or Vias in your STICKS diagram.

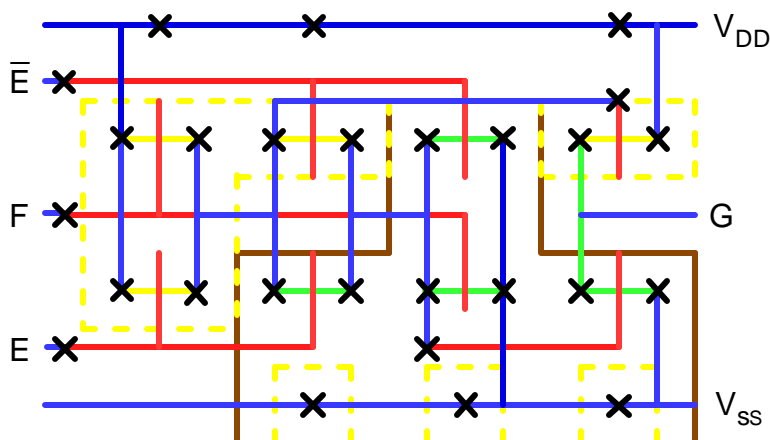
CMOS3DLM Layer	Color
N+ diffusion	Green
P+ diffusion	Yellow/Orange
P+ mask	Dotted Orange (outline)
P-Well	Solid Brown (outline)
Polysilicon	Red
Metal 1	Blue
Contact Cut	Black X
Metal 2	Black or Purple
Via	Black O

- b) Estimate the height (in design scale microns) of your STICKS diagram from part a). Some indication of the CMOS3DLM design rules you are using in your estimate must be given.

Three (3) popular solutions are shown for part a) and part b) on next three (3) pages. A detailed height estimate is shown only for solution 1).

Question #2 Work Sheet

Solution 1)



Height estimate:

Note the large amount of polysilicon. This should (will) cause some concern. Where used it increases the spacing around/between transistors.

Also note the following sizes (taken from bottom edge of diffusion to top edge of diffusion):

2 horizontal 1:1 n-channels = 29 dsm

2 horizontal 3:1 p channels = 45 dsm

1 horizontal 1:1 n-channel and 1 horizontal 3:1 p-channel = 43 dsm

1 vertical 1:1 n-channel and 1 vertical 3:1 p-channel = 79 dsm

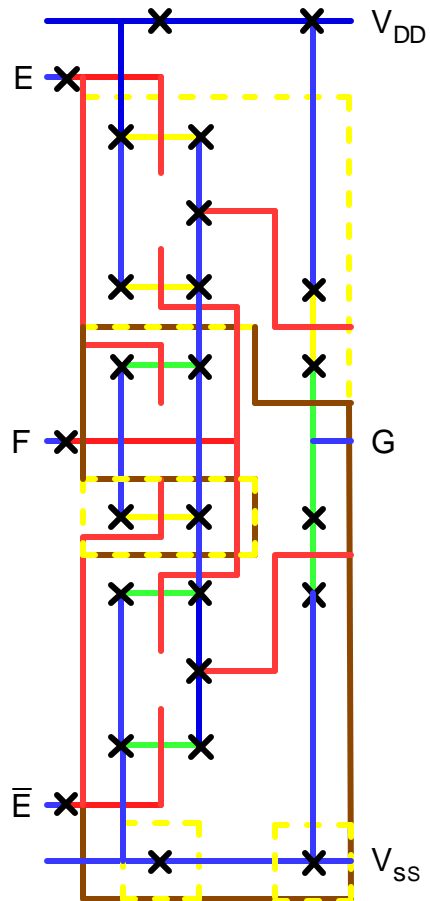
9	Vdd
5	metal spacing
9	metal- poly cut (using 9 instead of 11)
4	Poly-diffusion spacing
55	3:1 p to 3:1 p + 10 for poly inside
4	Poly-diffusion spacing
9	metal- poly cut (using 9 instead of 11)
5	metal spacing
9	Vss

Estimate Total: 109 dsm

Physical layout: 116 dms

Question #2 Work Sheet

Solution 2)



Height estimate:

Note the large amount of polysilicon. This should (will) cause some concern. Where used it increases the spacing around/between transistors.

Also note the following sizes (taken from bottom edge of diffusion to top edge of diffusion):

2 horizontal 1:1 n-channels = 29 dsm

2 horizontal 3:1 p channels = 45 dsm

1 horizontal 1:1 n-channel and 1 horizontal 3:1 p-channel = 43 dsm

1 vertical 1:1 n-channel and 1 vertical 3:1 p=channel = 79 dsm

Estimate Total: 220 dsm

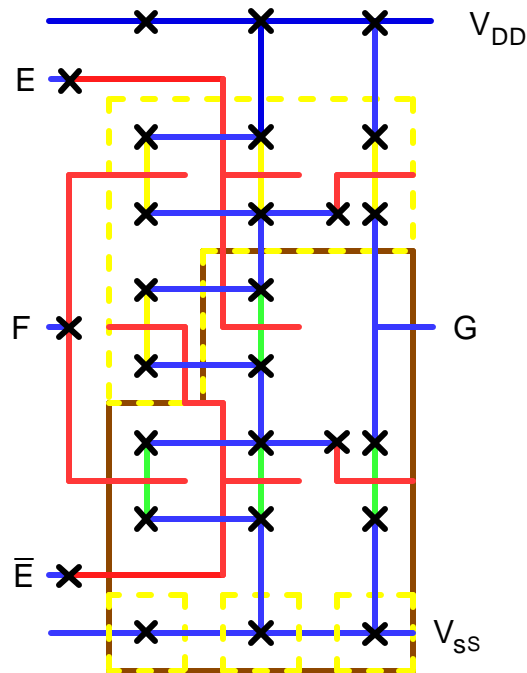
Physical layout: 230 dms

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Question #2 Work Sheet

Solution 3)



Height estimate:

Note the large amount of polysilicon. This should (will) cause some concern. Where used it increases the spacing around/between transistors.

Also note the following sizes (taken from bottom edge of diffusion to top edge of diffusion):

2 horizontal 1:1 n-channels = 29 dsm

2 horizontal 3:1 p channels = 45 dsm

1 horizontal 1:1 n-channel and 1 horizontal 3:1 p-channel = 43 dsm

1 vertical 1:1 n-channel and 1 vertical 3:1 p=channel = 79 dsm

5 metal spacing

5 metal width

9 metal-diffusion contact cut

11 metal-diffusion contact cut

Estimate Total: 181 dsm

Physical layout: 182 dms

QUESTION #3**MARKS: 15 (8 + 7)**

This question refers to the following logic equation:

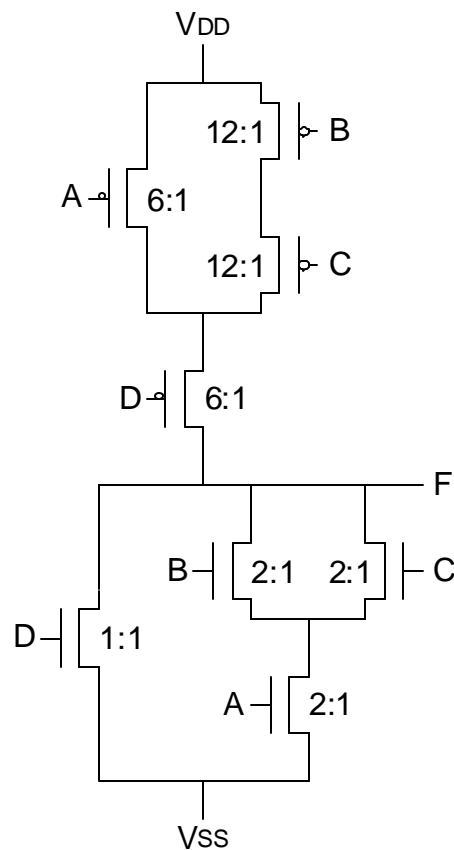
$$F = \overline{D + A \cdot (B + C)}$$

- a) Design a CMOS circuit to implement the logic function above using only eight (8) transistors. Draw a schematic diagram of your resulting circuit.

Design the pull-down circuit first, noting that the ACF will have a standard form since the output is inverted.

Note that OR operations are implemented with transistors in parallel. And that AND operations are implemented with transistors in series. AND operations have a higher binding than OR operations.

Note also that the pull-up circuitry is the dual of the pull-down circuitry.



- b) In order for the circuit designed in part a) to be as least as fast as a minimum size inverter (MSI), what must the sizes of the transistors be? Use the smallest size transistors as appropriate, assuming $\beta_n = 3\beta_p$. Clearly show the sizes (W:L) on a schematic diagram.

Always size transistors based upon the worst case pull-down and pull-up scenarios. Remember that the pull-down transistor in a MSI is 1:1 and the pull-up transistor in an MSI is 3:1.

Worst case pull-down scenarios are D or else A and B in series or else A and C in series.

Since D is by itself; therefore 1:1.

Since A and B are in series the transistors must be 2x as wide; therefore 2:1.

Since A and C are in series and A is already 2:1 then C must be 2x as wide; therefore 2:1.

Total transistor sizes pull-up (1:1, 2:1, 2:1, 2:1) = 7 widths

Worst case pull-up is D and A in series or else D and B and C in series.

Since D and A are in series the transistors must be 2x as wide; therefore 6:1.

Since D and B and C are in series and D is 6:1, the transistors for B and C must result in a 6:1 transistor width. Therefore the transistors are 4x as wide; therefore 12:1.

Total transistor sizes pull-up (6:1, 6:1, 12:1, 12:1) = 36 widths

Note: sizing D and B and C at 3x (9:1) and then sizing A the same may result in larger transistor sizes (i.e., if A is 3x then the effective pull-up (through A and D) is 4.5:1 which is a ratio that is higher than needed).

Total transistor sizes pull-up (9:1, 9:1, 9:1, 9:1) = 36 widths (same as above)

Extra Work Sheet

Student Name: _____

Student Number: _____